2015 European Conference on Circuit Theory and Design (ECCTD)

A digitally corrected bandgap voltage reference with a 3σ temperature coefficient of 3.8 ppm/K

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***Abstract*—Bangap voltage references (BGRs) are widely used in today's circuits as references with a low temperature coefficient. Especially measurement circuits and metering applications demand a very low temperature coefficient to maintain the desired precision over the entire temperature range. Today's BGR designs use analog circuits to correct for the effects which lead to a temperature drift. In this paper a bandgap reference voltage which uses a digital correction technique is presented. The proposed design includes a temperature sensor to measure the current chip temperature and a bandgap reference which is controllable by a 3-bit digital input. The input to the bandgap block is calculated using a digital correction algorithm.**

The proposed design was implemented in a 0.35 µm CMOS process and occupies 0.437 mm^2. After calibration, a 3σ temperature coefficient of 3.8 ppm/K is achieved over a temperature range from −40 °C to 100 °C.

With the proposed design, high performance measurements over a large temperature range have become possible. The digital design allows for an easy adaptation to various needs and temperature coefficients.

***Index Terms*—CMOS integrated circuits, Temperature dependence, Feedback circuits, Photonic band gap**

I. Introduction

Bandgap voltage references (BGRs) are essential blocks in most analog and mixed-signal circuits, such as analog-digital (AD) and digital-analog (DA) converters, voltage regulators, as well as measurement circuits. The goal of BGR design is to achieve a low temperature coefficient (TC) over a large temperature range. There are several approaches for curvature correction, such as quadratic [1] and high-order curvature compensation [2] or piece-wise linear curvature correction [3], [4]. Some bandgap reference designs include a heating element to keep the chip at an almost constant temperature at the cost of high current consumption [5]. An alternative approach is the use of floating gate architecture to create high precision, low power references [6]. As this relies on high voltage E^{2}PROM processes, such references are not an option for many designs. Current developments go towards more efficient trimming [7] or lower supply voltages [8], [9] often at the cost of a higher temperature coefficient.

A new approach for measurement circuits is presented in [10], where a digital temperature-dependent correction is applied. An AD converter with a BGR as reference voltage is used to digitize a measurement. A temperature sensor and a lookup table (LUT) are used to digitally estimate the errors introduced by the bandgap reference and compensate the digitized result for these errors. The bandgap block itself is not affected by the digital correction and thus still has a significant curvature.

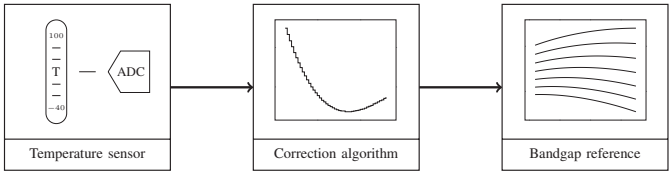

Fig. 1. Block diagram of proposed BGR

In this paper, a bandgap reference voltage design with a digitally corrected output voltage is presented. In comparison to [10], not only the digital measurement value, but the BGR block itself is corrected, which creates a temperature-stable reference voltage. This has the advantage that the operating point of e.g. a sensor and the measurement circuit are also stable over temperature.

II. Proposed Design

The proposed design consists of a temperature sensor with an analog-digital (AD) converter, a digital correction block and a bandgap reference. The block diagram of the proposed design is illustrated in Fig. 1. A digital temperature value is created by the temperature sensor and an integrated AD converter. Using this temperature value and programmable coefficients, a third order polynomial is evaluated. The corrected output value is then used to digitally control the bandgap reference block. In the following subsections, the different blocks of the design are discussed.

A. Temperature measurement

A digital temperature measurement is needed to calculate the correction value. In this paper, a simple temperature sensor is implemented by generating a temperature-constant reference current I_{ref} and a PTAT (proportional to absolute temperature) current I_{temp}. The difference of these two currents is digitized, using a first-order delta-sigma AD converter. The resolution of the temperature sensor is of particular significance for the design. A high resolution allows for a more accurate correction, but significantly increases the computational effort

978-1-4799-9877-7/15/$31.00

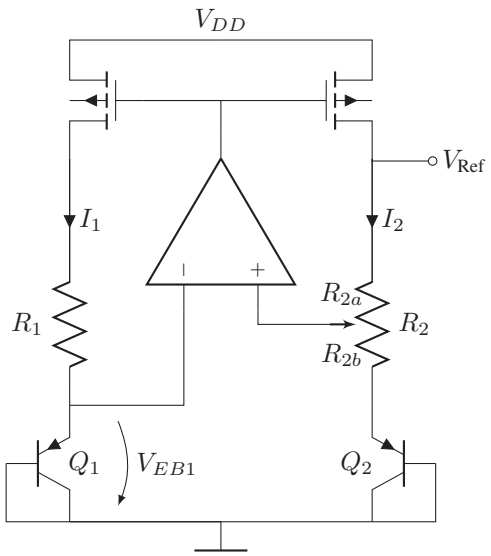

Fig. 2. Implementation of the BGR

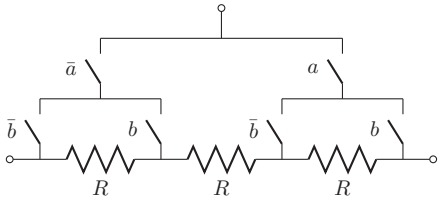

Fig. 3. Implementation of a 2 bit digitally controlled resistor R_2

and thus chip size and power consumption. In this design, a resolution of 6 bits is chosen as a trade-off between accuracy and computational effort.

As the error sources in the temperature sensor can be calibrated and compensated by the digital correction, the design of the temperature sensor is not of particular significance and is not further discussed here.

B. Design of bandgap reference

The bandgap reference block has a low temperature coefficient and can be digitally corrected. The schematic of the BGR is shown in Fig. 2. The transistors Q_1 and Q_2 each provide the emitter base voltage V_{EB}. The difference of the emitter-base voltages creates the PTAT term

$$\Delta V_{EB} = \Phi_T \ln\left(\frac{I_1 A_2}{I_2 A_1}\right) \tag{1}$$

where Φ_T is the thermal voltage kT/q, I_1 and I_2 are the emitter currents and A_1 and A_2 are the areas of the transistors Q_1 and Q_2. The resistor R_2 is realized as a cascade of resistors, as shown in Fig. 3. While the schematic only depicts a 2 bit controllable resistor, a 3 bit resistor cascade was implemented. This allows to control the ratio R_{2a}/R_{2b} using a digital signal. Thus R_2 can be interpreted as two independent resistors R_{2a} and R_{2b}. This results in the following formula

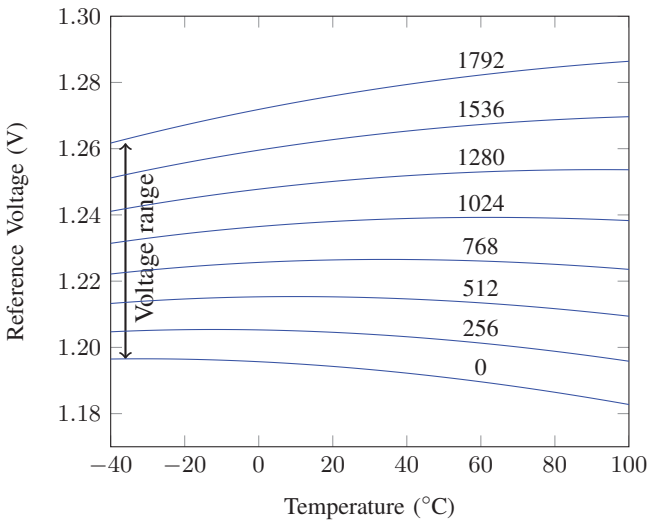

Fig. 4. Typical simulation of output voltages of bandgap reference

for V_{Ref}:

$$V_{\text{Ref}} = V_{EB1} + \Phi_T \ln\left(\frac{I_1 A_2}{I_2 A_1}\right) \frac{R_{2a}}{R_{2b}} \tag{2}$$

Both transistors Q_1 and Q_2 are chosen to have the same size, i.e. $A_1 = A_2$. Further the resistors R_1 and R_2 are implemented identically, thus $R_1 = R_2$. This allows for the implementation of a chopping between the two currents I_1 and I_2 and thus the compensation of mismatches between the two paths and the offset of the operational amplifier. Further the currents I_1 and I_2 are generated as $I_1 = 7I_2$ using an element rotating strategy as shown in [11].

The resistor cascade R_2 is constructed such that the ratio R_{2a}/R_{2b} can be controlled by a 3-bit digital input. This leads to 8 possible values for the output voltage V_{ref}, each with a different temperature drift. A typical simulation of the output voltages is shown in Fig. 4.

C. Digital correction algorithm

A digital correction algorithm can now be designed to create a constant output voltage within the marked voltage range in Fig. 4.

1) Pulse density modulation: The precision of 3 bit for the resistor cascade R_2 is too small to achieve a low temperature coefficient. To increase precision, the resistor cascade is controlled by a pulse density modulated (PDM) signal. The correction value K, which is put onto R_2 as PDM signal is chosen to have a width of 11 bit. The maximal possible value for K is therefore $111\,0000\,0000_{\text{bin}}$ or 1792_{dec}, as indicated in Fig. 4. The PDM block is shown in Fig. 5 It is apparent that the PDM introduces switching noise, thus an external lowpass filter is required to reduce noise.

2) Calculation of correction value: It was shown by simulation that the approximation of the output curves as polynomials of third order leads to errors which are smaller than the switching effects of the digital correction. The 11-bit

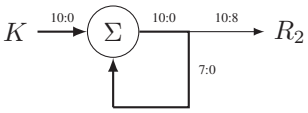

Fig. 5. Pulse density modulator

correction value K which will be used to set the PDM signal can therefore be calculated as follows:

$$K = ((a_3 t + a_2)\, t + a_1)\, t + a_0 \tag{3}$$

where t is the digital 6 bit temperature value. The coefficients a_i are estimated by simulating or measuring the output voltages of the BGR, as depicted in Fig. 4. From this, the optimal coefficients which lead to a constant output voltage V_{Ref} can be calculated and used to calibrate the BGR.

The coefficients a_i for a typical simulation are

$$a_3 = -0.029 \quad a_2 = 0.465 \quad a_1 = 21.49 \quad a_0 = 1345$$

3) Evaluation of polynomial: For an efficient implementation, the calculation has to be performed using fixed-point arithmetic. As the values of the coefficients $a_3, \ldots, a_0$ differ by factors of more than 10, they are scaled for a more efficient calculation. A scaling of 2^{-5} per stage is chosen as a trade-off between accuracy and computational effort. This leads to the implemented digital correction algorithm

$$K = \left(\left(p_3 2^{-5} t + p_2\right) 2^{-5} t + p_1\right) 2^{-5} t + p_0 \tag{4}$$

where p_i are the scaled versions of the coefficients a_i

$$p_i = a_i \cdot 2^{5i} \quad \text{for } i \in \{0, 1, 2, 3\} \tag{5}$$

The evaluation of the polynomial is implemented using Booth's algorithm for signed multiplication [12]. To handle negative coefficients and thus negative intermediate results the two's complement is used. The MAC units are designed to have a word width of 12 bits. As the result of the polynomial (4), i.e. the correction value K, must always be positive, the MSB of the two's complement value is ignored, which leads to the 11-bit correction value K.

4) Simulation: A typical simulation of the proposed bandgap reference system for a voltage of $V_{\text{Ref}} = 1.24V$ is shown in Fig. 6. The simulated temperature coefficient is as low as 2.78 ppm/K for the temperature range from –40 °C to 100 °C.

III. Experimental Results

The proposed bandgap reference design has been implemented in the *AMS C35* 0.35 µm CMOS technology and occupies 0.437 mm^2 of core area. Fig. 7 shows a micrograph of the chip. The digital part contains the described correction algorithm, as well as the control for the temperature sensor and the delta modulator to control the BGR. Further, an SPI serial interface was implemented to read/write the coefficients p_i and the measured temperature value. The digital part takes up most of the chip area, while the bandgap block only needs as little as 0.023 mm^2 of chip area. The use of a CMOS process with a smaller feature size would thus allow for substantial reduction of the chip area.

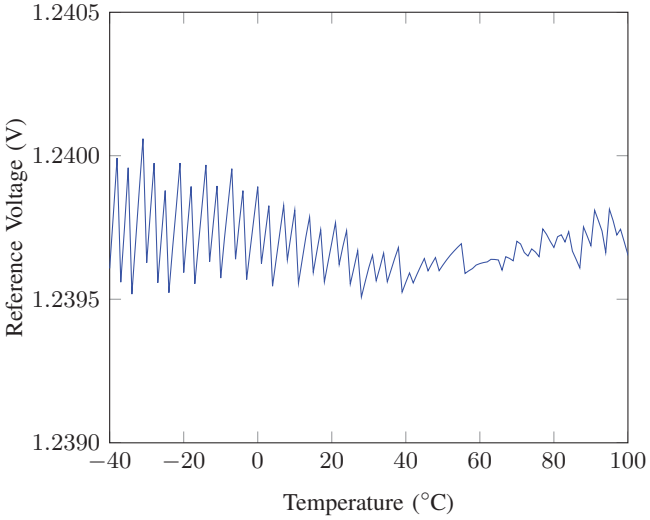

Fig. 6. Typical simulation of corrected output voltage

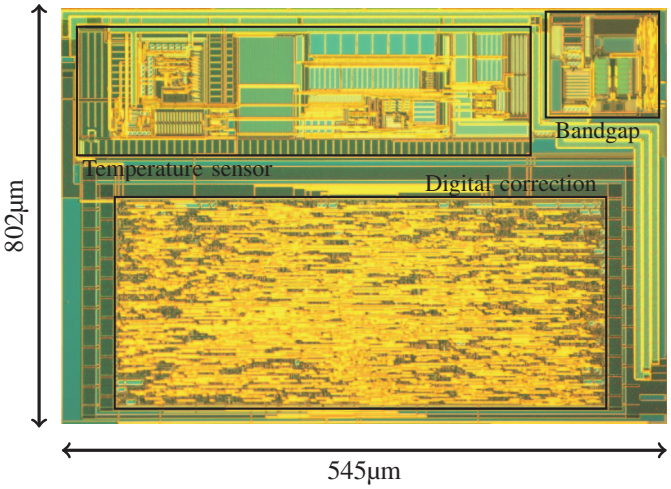

Fig. 7. Micrograph of the proposed bandgap voltage reference

The clock frequency for the chopping as well as the digital part is chosen to be 100 kHz. Due to the chopping and the pulse density modulation, an external lowpass filter has to be added for noise reduction. In this measurement setup, a capacitor of 47 nF is used.

A. Calibration

The calibration of the proposed bandgap reference design is achieved by programming the coefficients of the correction polynomial (4). As a third order polynomial is used, at least four measurements at different temperatures are needed for the calculation of the coefficients. Best results are achieved by distributing the measurement temperatures over the entire temperature range. At each measurement point, the output voltages of the bandgap block are measured. Interpolation by

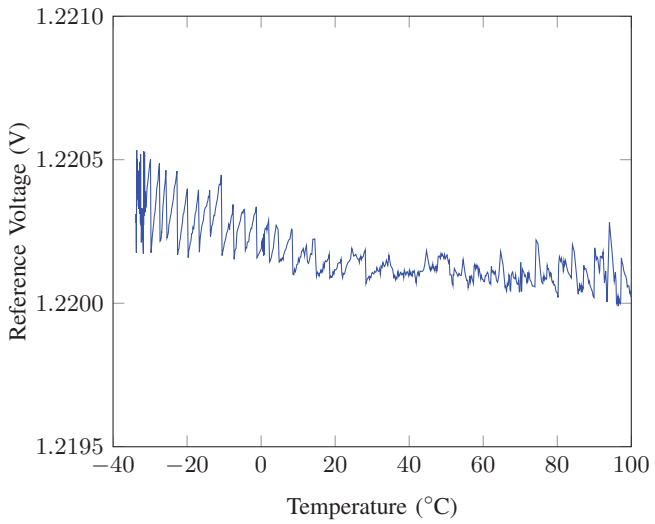

Fig. 8. Measurement of corrected output voltage

a third order polynomial then leads to curves similar to Fig. 4. The coefficients of the optimal correction polynomial can then be calculated and written onto the BGR chip.

B. Results

A series of five chips in a plastic package was calibrated and measured and the simulated results could be verified. The resulting corrected output voltage of one chip within the range of −40 °C to 100 °C is shown in Fig. 8. The temperature coefficients of the measured chips vary between 2.89 ppm/K and 3.44 ppm/K for an output voltage of $V_{\text{ref}} = 1.22\,\text{V}$. The 3σ temperature coefficient is 3.8 ppm/K. At room temperature (26 °C), the supply current is 53 µA at $V_{DD} = 3.3\,\text{V}$. The noise introduced by the BGR is $0.15\,\mu\text{V}/\sqrt{\text{Hz}}$ @ 1 kHz.

The performance of the proposed bandgap reference design compared to previously published bandgap references is summarized in Table I. The digitally corrected bandgap reference features the lowest temperature coefficient at the cost of a larger chip area. However it should be pointed out that the chip area is mostly determined by the size of the digital part, which can easily be reduced by technology scaling.

IV. Conclusions

In this paper, a novel bandgap reference design using a digital correction algorithm has been presented. The digital design comes with a large flexibility and allows for an easy adaptation of this BGR design to various requirements. The proposed design has been implemented in a 0.35 µm CMOS technology and achieves a 3σ temperature coefficient of 3.8 ppm/K over the temperature range from −40 °C to 100 °C.

As the current design requires at least four measurements at different temperatures, the calibration is expensive. Further efforts will be put into the development of a calibration scheme to reduce the number of measurements to ideally one measurement at room temperature.

TABLE I
Comparison of bandgap voltage references

Parameter	**This work**	[2]	[7]	[10]
Reference voltage (V)	1.220	1.142	1.0875	1.215
Temperature range (°C)	−40 to 100	0 to 100	−40 to 125	−40 to 125
Temperature coefficient (ppm/K)	**3.8**	5.3	12	7
Noise	$0.15\,\frac{\mu\text{V}}{\sqrt{\text{Hz}}}$ @ 1 kHz	$0.12\,\frac{\mu\text{V}}{\sqrt{\text{Hz}}}$ @ 1 kHz	$6.3\,\mu\text{V}_{\text{RMS}}$ 0.1–10 Hz	n.a.
Supply current (µA)	53	23	55	10.5
Technology	0.35 µm	0.6 µm	0.16 µm	0.13 µm
Chip area (mm^2)	0.437	0.057	0.120	0.034

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